A SACRIFICIAL TiN ARC LAYER FOR INCREASED PAD ETCH THROUGHPUT

Jeffrey A. Shields
Kelwin Ko

ABSTRACT

A method of manufacturing a semiconductor device wherein a final layer of metal is formed on a layer of interlayer dielectric, forming a layer of TiN on the final layer of metal, forming a layer of photoresist on the layer of TiN, patterning and developing the layer of photoresist exposing portions of the final metal layer, and etching the exposed portions of the final metal layer forming metal structures. The layer of photoresist and layer of TiN are removed. A blanket layer of interlayer dielectric is formed on the surface of the semiconductor device. A second layer of photoresist is formed on the blanket layer of interlayer dielectric. The second layer of photoresist is patterned and developed exposing portions of the interlayer dielectric overlying the metal structures. The exposed portions of the interlayer dielectric are etched down to the surface of the metal structures.